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# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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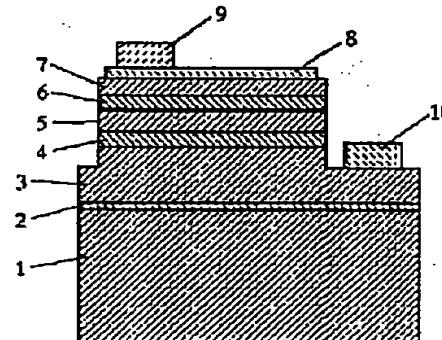
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TITLE : NITRIDE SEMICONDUCTOR ELEMENT  
AND GROWING METHOD OF NITRIDE  
SEMICONDUCTOR



ABSTRACT : PROBLEM TO BE SOLVED: To mainly increase the outputs of an LED and an LD by arranging a second nitride semiconductor layer, wherein p-type impurities are gradually reduced further it is from a first nitride semiconductor layer, on the first nitride semiconductor layer.

SOLUTION: A second p-type nitride semiconductor layer 6 which is slantly doped with p-type impurities is formed on a first nitride semiconductor layer 5. The light-emitting element output can be increased by slantly doping the second p-type nitride semiconductor layer 6 with p-type impurities. That is, the output of the whole element can be increased by arranging a third p-type nitride semiconductor, which acts as a contact layer and is doped with p-type impurities of high concentration, a second p-type nitride semiconductor which is doped with p-type impurities in a position more adjacent to an active layer 4 than the third p-type nitride semiconductor layer 7, and a first nitride semiconductor which is doped with p-type impurities of high concentration in a position more adjacent to the active layer 4 than the second nitride semiconductor.

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**[Claim(s)]**

**[Claim 1]** The 1st nitride semiconductor layer which contains p type impurity in the barrier-layer upper part is formed. in the 1st nitride semiconductor layer upper part It has the 2nd nitride semiconductor layer whose p type high impurity concentration is decreasing gradually as it separates from the 1st nitride semiconductor layer. The nitride semiconductor device characterized by having the 3rd nitride semiconductor layer which contains a lot of p type impurities than an average of p type high impurity concentration of the 2nd nitride semiconductor layer in the 2nd nitride semiconductor layer upper part.

**[Claim 2]** The nitride semiconductor device according to claim 1 to which the nitride semiconductor layer of the above 2nd is characterized by for two or more nitride semiconductor layers having consisted of a multilayer by which the laminating was carried out, and p type impurity of the multilayer having decreased gradually.

**[Claim 3]** The source of p type impurity after growing up the 1st nitride semiconductor layer which contains p type impurity using the source gas of p type impurity, III \*\*\*\* gas, and nitrogen source gas in a reaction container, By growing up the 2nd nitride semiconductor layer using III \*\*\*\* gas and nitrogen source gas, and reducing gradually the flow rate of the source gas of p type impurity during the 2nd nitride semiconductor growth The growth method of the nitride semiconductor characterized by making it decrease as p type high impurity concentration in the 2nd nitride semiconductor layer is separated from the 1st nitride semiconductor layer.

**[Detailed Description of the Invention]****[0001]**

**[Industrial Application]** this invention relates to the growth method of the nitride semiconductor which constitutes the element which consists of a nitride semiconductor ( $\text{In}_X\text{Al}_Y\text{Ga}_{1-X-Y}\text{N}$ ,  $0 \leq X, Y \leq 1$ ,  $X+Y \leq 1$ ) used for photo detectors, such as light emitting devices, such as Light Emitting Diode and LD, a solar battery, and a photosensor, etc., and its element.

**[0002]**

**[Description of the Prior Art]** The nitride semiconductor was just put in practical use by these people with the full color Light Emitting Diode display, the traffic light, etc. as a material of high brightness blue Light Emitting

Diode and authentic green Light Emitting Diode. Light Emitting Diode used for these various devices has terrorism structure to the double by which the barrier layer which consists of InGaN of single quantum well structure (SQW:Single-Quantum-Well) was sandwiched between n type nitride semiconductor layer and p type nitride semiconductor layer. Wavelength, such as blue and green, is determined by fluctuating In composition ratio of an InGaN barrier layer. Blue Light Emitting Diodes are the luminescence wavelength of 450nm, the half-value width of 20nm, the luminous intensity of 2 cds, 5mW of optical outputs, and 9.1% of external quantum efficiencies in 20mA. On the other hand, similarly green Light Emitting Diodes are the luminescence wavelength of 525nm, the half-value width of 30nm, the luminous intensity of 6 cds, 3mW of optical outputs, and 6.3% of external quantum efficiencies in 20mA.

[0003] Moreover, these people announced the 410nm laser oscillation in a room temperature for the first time under the pulse current in the world recently using this material {Jpn.J.Appl.Phys.35(1996) L74 and Jpn.J.Appl.Phys.35(1996) L217 grade}. This laser element has terrorism structure to the double which has the barrier layer of multiplex quantum well structure which used InGaN, is the conditions of 2 microseconds of pulse width, and 2ms of pulse periods, and shows the oscillation of the threshold current of 610mA, and threshold current density 8.7 kA/cm<sup>2</sup>, 410nm. The improved laser element was also announced in Appl.Phys.Lett.69 (1996) 1477. This laser element has the structure where the ridge stripe was formed in a part of p type nitride semiconductor layer, is 1 microsecond of pulse width, 1ms of pulse periods, and 0.1% of duty ratio, and shows the oscillation of the threshold current of 187mA, and threshold current density 3 kA/cm<sup>2</sup>, 410nm. Furthermore, these people succeeded also in the continuous oscillation in a room temperature for the first time, and announced. A this {Nikkei electronics December 2, 1996 issue technical news flash [ for example, ], Appl.Phys.Lett.69 (1996) 3034, Appl.Phys.Lett.69 (1996) 4056, etc. and laser} element shows the continuous oscillation of 27 hours in 20 degrees C in threshold current density 3.6 kA/cm<sup>2</sup> and a threshold-voltage 5.5V or 1.5mW output.

[0004]

[Problem(s) to be Solved by the Invention] Thus, although the luminescence

device using the nitride semiconductor is already put in practical use as a Light Emitting Diode, there is also a still inadequate point and improvement in the further radiant power output is desired. Moreover, LD is under research wholeheartedly now aiming at utilization, and reinforcement is desired not to mention improvement in an output. If the radiant power output of a luminescence device like these [ Light Emitting Diode and LD ] can be raised, the light-receiving efficiency of light-receiving devices, such as a solar battery and a photosensor, in which it has similar structure can also be raised simultaneously. Therefore, the place which accomplishes this invention in view of such a situation, and is made into the purpose is by offering the structure of a new nitride semiconductor device, and the growth method of the nitride semiconductor which constitutes the nitride semiconductor device to mainly raise the output of Light Emitting Diode and LD.

[0005]

[Means for Solving the Problem] The 1st nitride semiconductor layer to which the nitride semiconductor device of this invention contains p type impurity in the barrier-layer upper part is formed. The 1st nitride semiconductor layer upper part is equipped with the 2nd nitride semiconductor layer whose p type high impurity concentration is decreasing gradually as it separates from the 1st nitride semiconductor layer. It is characterized by having the 3rd nitride semiconductor layer which contains p type impurity of more amounts than an average of p type high impurity concentration of the 2nd nitride semiconductor layer in the 2nd nitride semiconductor layer upper part. In addition, in this invention, a barrier layer and the 1st nitride semiconductor layer touch, and it does not need to be formed, and the 1st nitride semiconductor layer and the 2nd nitride semiconductor layer touch, and it does not need to be formed, and further, the 2nd nitride semiconductor layer and the 3rd nitride semiconductor layer touch, and do not need to be formed.

[0006] Furthermore, the nitride semiconductor device of this invention consists of a multilayer to which the laminating of the nitride semiconductor layer of plurality [ layer / nitride semiconductor / of the above 2nd ] was carried out, and it is characterized by p type impurity of the multilayer having decreased gradually.

[0007] The growth method of the nitride semiconductor of this invention is set in a reaction container. The source gas of p type impurity, The source of p type impurity after growing up the 1st nitride semiconductor layer containing p type impurity using III \*\*\*\* gas and nitrogen source gas, By growing up the 2nd nitride semiconductor layer using III \*\*\*\* gas and nitrogen source gas, and reducing gradually the flow rate of the source gas of p type impurity during the 2nd nitride semiconductor growth It is characterized by making it decrease as p type high impurity concentration in the 2nd nitride semiconductor layer is separated from the 1st nitride semiconductor layer.

[0008]

[Embodiments of the Invention] Drawing 1 is the typical cross section showing the structure of the nitride semiconductor device concerning one example of this invention, and specifically shows the structure of a Light Emitting Diode element. The buffer layer 2 which consists of GaN as element structure on the substrate 1 which consists of sapphire, the n side contact layer 3 (\*\* n side clad layer) which consists of an Si dope GaN, The barrier layer 4 which consists of InGaN of the single quantum well structure of 30A of thickness, The 1st p side nitride semiconductor layer 5 which consists of a Mg dope AlGaN, It has come to carry out the laminating of the 2nd p side nitride semiconductor layer 6 which Mg becomes from GaN by which the inclination dope was carried out, and the 3rd p side nitride semiconductor layer 7 which Mg average concentration becomes from doped GaN. Mostly, the p electrode 8 of the 3rd p side nitride semiconductor layer 7 which becomes the whole surface from the metal thin film of a translucency is formed, and the pad electrode 9 for bondings is formed in the corner of the whole surface electrode 8. The n electrode 10 is formed in the front face of the n side contact layer 3 \*\*\*\*\*ed and exposed from the p side nitride semiconductor layer side on the other hand.

[0009] Moreover, the data which analyzed this Light Emitting Diode element by SIMS (secondary-ion-mass-spectroscopy equipment) to drawing 2 are shown. Mg shows concentration, and secondary ionic strength has and shows In. That is, In peak shows the position of a barrier layer and it is shown that Mg is distributed over the p layer side rather than the barrier layer. In this drawing, the spatter of the Light Emitting Diode element is carried out with

Cs ion from the best layer, and the element which comes out is analyzed, and the depth is taken along a horizontal axis, Mg concentration and In intensity are taken along a vertical axis, and it is shown. Thus, with the element of this invention, it has the nitride semiconductor layer adjusted so that it might become small gradually as Mg concentration separates from a barrier layer.

[0010] With the element of this invention, it has the 2nd p side nitride semiconductor layer 6 by which the inclination dope of the p type impurity was carried out on the 1st nitride semiconductor layer 5 containing p type impurity. By carrying out the inclination dope of the p side impurity in this way, this 2nd p side nitride semiconductor layer can raise a light-emitting-device output. Namely, the 3rd p side nitride semiconductor with which p type impurity which acts as a contact layer was doped by high concentration, The 2nd p side nitride semiconductor with which the inclination dope of the p type impurity was carried out in the position which approached the barrier layer rather than the 3rd p side nitride semiconductor layer, Since it can be made easy to accumulate in a barrier layer, the carrier poured in from a contact layer side when p type impurity equips the position which furthermore approached the barrier layer rather than the 2nd nitride semiconductor with the 1st p side nitride semiconductor doped at high concentration The output of the whole element can be raised.

[0011] A barrier layer 4 is taken as the single quantum well structure containing the nitride semiconductor layer which contains In at least, or multiplex quantum well structure. As for a well layer, it is [ 100A or less of thickness ] still more preferably desirable to constitute from  $InXGa1-XN$  ( $0 < X \leq 1$ ) 70A or less, and, as for a barrier layer, it is desirable to constitute still more preferably  $InYGa1-YN$  ( $0 < Y \leq 1$ ) with larger bandgap energy than a well layer or 200A or less of  $AlX'Ga1-X'N$  ( $0 < X' \leq 1$ ) from thickness 150A or less.

[0012] That what is necessary is just to consist of nitride semiconductor layers containing p type impurity, even if the 1st p side nitride semiconductor layer 5 is in contact with especially the barrier layer, it does not need to be. The large nitride semiconductor of bandgap energy is chosen from a barrier layer as a semiconductor, for example,  $AlXGa1-XN$  ( $0 \leq X \leq 1$ ) is grown up preferably as mentioned above. p type high impurity concentration doped on the other hand is adjusted to three or more  $5 \times 10^{18}$

/cm and  $5 \times 10^{20}$  /cm<sup>3</sup> still more preferably three or more  $1 \times 10^{18}$  /cm and three or less  $1 \times 10^{21}$  /cm. As a p type impurity, II group elements, such as Mg, Zn, Cd, calcium, Be, and Sr, are doped preferably. Furthermore, two kinds of nitride semiconductor layers from which composition differs mutually can also use this 1st nitride semiconductor layer as the superlattice layer which comes to carry out a laminating. When considering as a superlattice layer, 100A or less of 70A or less of thickness of the nitride semiconductor layer which constitutes a superlattice layer is most preferably adjusted to thickness 50A or less still more preferably. If it is a superlattice layer, the crystallinity of a nitride semiconductor layer will become good and an output will improve further. When considering as a superlattice layer, p type impurity may be doped in both layers, and may be doped in one of layers.

[0013] Although it is desirable to be formed in contact with the 1st nitride semiconductor layer 5 as for the 2nd nitride semiconductor layer 6, it does not need to be touched and formed especially. For example, the nitride semiconductor layer of undoping of thickness hundreds of A or less can also be grown up between the 1st and the 2nd nitride semiconductor layer. Moreover, although it is desirable to adjust so that the 3rd nitride semiconductor layer 6 may be approached and it may decrease continuously as for an impurity, the amount of dopes of p type impurity can be lessened gradually, and the 2nd nitride semiconductor layer can also be grown up. Although especially composition of a nitride semiconductor layer is not asked, it is preferably considered as the same composition as the 3rd nitride semiconductor layer. 2 micrometers or less of 1 micrometer or less of thickness of the 2nd nitride semiconductor layer are most preferably adjusted to 0.5 micrometers or less still more preferably. Moreover, you may make p type high impurity concentration of the nitride semiconductor layer which constitutes the multilayer for the 2nd nitride semiconductor layer as multilayer (superlattice is included) structure of a nitride semiconductor decrease gradually.

[0014] If it is desirable to consider as the contact layer which forms p electrode as for the 3rd nitride semiconductor layer 7 and X value sets to 0.3 or less Al<sub>X</sub>Ga<sub>1-X</sub>N ( $0 \leq X \leq 0.3$ ) preferably, p electrode and desirable OMIKKU will be obtained. As for p type high impurity concentration of the 3rd nitride semiconductor layer 7, it is desirable to adjust to three or more

5x10<sup>18</sup>/cm and 5x10<sup>20</sup>/cm<sup>3</sup> still more preferably as well as the 1st nitride semiconductor layer 5 three or more 1x10<sup>18</sup>/cm and three or less 1x10<sup>21</sup>/cm. Moreover, as for the thickness of the 3rd nitride semiconductor layer, it is desirable to adjust more thinly than the 2nd nitride semiconductor layer. That is, thickness of 3rd p type nitride semiconductor layer which acts as a contact layer is made thin, and since contact resistance falls by doping p type impurity to high concentration, it is in the inclination for Vf (forward voltage) to tend to fall.

[0015]

[Example] Hereafter, the manufacture method of the nitride semiconductor device of this invention is explained using the MOCVD method.

[0016] The substrate which makes a [example 1] sapphire (0001) side a principal plane is prepared, and the buffer layer which uses TMG (trimethylgallium) and ammonia for material gas, and consists of GaN at 500 degrees C is grown up by 200A thickness.

[0017] Next, temperature is raised at 1050 degrees C, mono-silane gas is used for TMG, ammonia, and impurity gas, and the n type GaN layer which doped Si 1x10<sup>19</sup>/cm<sup>3</sup> is grown up by 5-micrometer thickness.

[0018] Next, temperature is made into 800 degrees C and the well layer which consists of undoping In0.4Ga0.6N is grown up by 25A thickness as a barrier layer using TMI (trimethylindium), TMG, and ammonia.

[0019] Next, temperature is made into 1050 degrees C and the 1st nitride semiconductor layer which consists of p type aluminum0.3Ga0.7N which doped Mg 1x10<sup>20</sup>/cm<sup>3</sup> is grown up by 200A thickness, using Cp2Mg (magnesium cyclopentadienyl) as TMG, ammonia, and impurity gas. This 1st nitride semiconductor layer acts as a layer which shuts up a carrier.

[0020] Material gas is stopped after the 1st nitride semiconductor layer growth, TMG, ammonia, and Cp2Mg are poured again continuously, and the 2nd nitride semiconductor layer which p type impurity becomes from GaN by which the inclination dope was carried out at 1050 degrees C is grown up by 0.18-micrometer thickness. However, when MFC (mass-flow controller) adjusts Cp2Mg so that a flow rate may decrease gradually during growth, and the 2nd nitride semiconductor finishes growing, it is made for the flow rate of Cp2Mg to be set to 0.

[0021] The 3rd nitride semiconductor layer which doped Mg 1x10<sup>20</sup>/cm<sup>3</sup> is

grown up by 300A thickness after the 2nd nitride semiconductor layer growth using TMG, ammonia, and Cp2Mg.

[0022] Annealing is performed for the wafer into which the nitride semiconductor was grown up as mentioned above at 700 degrees C among nitrogen atmosphere in a reaction container, and the layer which doped p type impurity is made to form into low resistance further. A wafer is picked out from a reaction container after annealing, an RIE system performs etching from a 3rd [ of the best layer ] nitride semiconductor layer side, and the front face of the n side contact layer which should form n electrode is exposed. Mostly, the whole surface electrode of the 3rd nitride semiconductor layer of the best layer which becomes the whole surface from nickel/Au is formed by 200A thickness, and the pad electrode which turns into a part of the whole surface electrode from Au by 1-micrometer thickness is formed. On the other hand, n electrode which consists of W and Au is formed in the front face of the exposed n side contact layer.

[0023] When it separated into the chip of 350-micrometer angle and the wafer which formed the electrode as mentioned above was made to emit light, in 20mA, it became Vf3.2V, the luminescence wavelength of 525nm, 3.5mW of optical outputs, and 7.3% of external quantum efficiencies, and improved by about 1.2 times as compared with the conventional green Light Emitting Diode which has not carried out an inclination dope.

[0024] In the [example 2] example 1, material gas is stopped after the 1st nitride semiconductor layer growth, and TMG, ammonia, and Cp2Mg are poured again continuously. at 1050 degrees C 500A of GaN layers which doped p type impurity  $1 \times 10^{19}/\text{cm}^3$  is grown up. Next, change the flow rate of Cp2Mg and 500A of GaN layers which doped Mg  $5 \times 10^{18}/\text{cm}^3$  is grown up. Next, 500A of GaN layers which doped Mg  $1 \times 10^{18}/\text{cm}^3$  is grown up, 500A of GaN layers which finally have not doped Mg is grown up, and the 2nd nitride semiconductor layer of the 0.2 micrometers of the total thickness is grown up. When others were made to be the same as that of an example 1, they have produced the Light Emitting Diode element which has a property almost equivalent to the thing of an example 1.

[0025] [Example 3] drawing 3 is the typical cross section showing the structure of the 1 laser element concerning this invention, and explains the 3rd example of this invention hereafter based on this drawing.

[0026] The GaN substrate 100 into which the single crystal which consists of GaN through the buffer layer which consists of GaN on the substrate which makes a sapphire (0001) side a principal plane was grown up by 120-micrometer thickness is prepared. In the state where it was made to grow up on sapphire, this GaN substrate 100 is set in a reaction container, temperature is raised to 1050 degrees C, and the n side buffer layer 11 which consists of GaN which doped Si  $1 \times 10^{18}/\text{cm}^3$  on the GaN substrate 100 like an example 1 is grown up by 4-micrometer thickness. This n side buffer layer is a buffer layer grown up at an elevated temperature, for example, the buffer layer 2 which grows up GaN, AlN, etc. directly by thickness 0.5 micrometers or less in low temperature 900 degrees C or less on the substrate which consists of sapphire, SiC, and a different material from a nitride semiconductor like a spinel like an example 1 is distinguished.

[0027] (n side clad layer 12= strained super lattice layer) Then, the 1st layer which consists of n type aluminum $0.3\text{Ga}0.7\text{N}$  which doped Si  $1 \times 10^{19}/\text{cm}^3$  using TMA, TMG, ammonia, and silane gas at 1050 degrees C is grown up by 40A thickness, silane gas and TMA are stopped continuously and the 2nd layer which consists of GaN of undoping is grown up by 40A thickness. and 1st layer + 2nd layer + 1st layer + 2nd layer + -- like ..., a strained super lattice layer is constituted, the laminating of every 100 layers is carried out by turns, respectively, and the n side clad layer 12 which consists of a strained super lattice of the 0.8 micrometers of the total thickness is grown up

[0028] (n photometry guide layer 13) Then, silane gas is stopped and n photometry guide layer 13 which consists of undoping GaN at 1050 degrees C is grown up by 0.1-micrometer thickness. As for this n photometry guide layer, it is desirable to act as a light-guide layer of a barrier layer, and to grow up GaN and InGaN, and it is usually desirable to make it grow up by 200A - 1 micrometer thickness still more preferably 100A - 5 micrometers. Moreover, it can also consider as the strained super lattice layer of undoping of this layer. In considering as a strained super lattice layer, bandgap energy is larger than a barrier layer, and it makes it smaller than the n side clad layer.

[0029] (Barrier layer 14) Next, TMG, TMI, and ammonia are used for material gas, and a barrier layer 14 is grown up. A barrier layer 14 holds

temperature at 800 degrees C, and grows up the well layer which consists of undoping In<sub>0.2</sub>Ga<sub>0.8</sub>N by 25A thickness. Next, the barrier layer which consists of undoping In<sub>0.01</sub>Ga<sub>0.95</sub>N at the same temperature only by changing the mole ratio of TMI is grown up by 50A thickness. This operation is repeated twice and the barrier layer of the multiplex quantum well structure (MQW) of the 175A of the total thickness which carried out the laminating of the well layer to the last is grown up. Undoping is sufficient as a barrier layer like this example, and it may dope n type impurity and/or p type impurity. An impurity may be doped to both a well layer and a barrier layer, and may be doped to either.

[0030] (p side cap layer 15= 1st nitride semiconductor layer) Next, temperature is raised to 1050 degrees C and the p side cap layer 17 which consists of p type aluminum<sub>0.3</sub>Ga<sub>0.7</sub>N with larger bandgap energy which doped Mg  $1 \times 10^{20}$ /cm<sup>3</sup> than p photometry guide layer 16 is grown up by 300A thickness using TMG, TMA, ammonia, and Cp<sub>2</sub>Mg (magnesium cyclopentadienyl). If the p side cap layer is preferably grown up into 0.5 micrometers or less and a further by thickness 0.1 micrometers or less, since it will act as barrier for the p side cap layer shutting up a carrier in a barrier layer, its output improves. Although especially the minimum of the thickness of this p type cap layer 15 does not limit, it is desirable to form by thickness 10A or more.

[0031] (p photometry guide layer 16= 2nd nitride semiconductor layer) p photometry guide layer 16 which p type impurity with bandgap energy smaller than the p side cap layer 15 becomes from GaN by which the inclination dope was carried out at 1050 degrees C like an example 1 after p side cap layer 15 growth using TMG, Cp<sub>2</sub>Mg, and ammonia again is grown up by 0.1-micrometer thickness. This layer acts as a light-guide layer of a barrier layer.

[0032] (p side clad layer 17) Then, the 3rd layer which consists of p type aluminum<sub>0.3</sub>Ga<sub>0.8</sub>N which doped Mg  $1 \times 10^{20}$ /cm<sup>3</sup> at 1050 degrees C is grown up by 40A thickness, only TMA is stopped continuously and the 4th layer which consists of undoping GaN is grown up by 40A thickness. And this operation is repeated 100 times, respectively and the p side clad layer 17 which consists of a strained super lattice layer of the 0.8 micrometers of the total thickness is formed.

[0033] (p side contact layer 18= 3rd nitride semiconductor layer) The p side contact layer 18 which finally consists of p type GaN which doped Mg  $2 \times 10^{20}$ /cm<sup>3</sup> on the p side clad layer 17 at 1050 degrees C is grown up by 150A thickness. The p side contact layer 18 can be constituted from p type In<sub>X</sub>Al<sub>Y</sub>Ga<sub>1-X-Y</sub>N ( $0 \leq X, Y \leq 1, X+Y \leq 1$ ), and GaN which doped Mg preferably, then the p electrode 21 and the most desirable ohmic contact are obtained. Moreover, since the p side clad layer 17 of the strained super lattice structure containing p mold AlYGa<sub>1-Y</sub>N is touched and the thickness is made thin with 500A or less by using the small nitride semiconductor of bandgap energy as the p side contact layer, the carrier concentration of the p side contact layer 18 becomes high substantially, p electrode and desirable OMIKKU are obtained, and the threshold current of an element and voltage fall.

[0034] Annealing is performed for the wafer into which the nitride semiconductor was grown up as mentioned above at 700 degrees C among nitrogen atmosphere in a reaction container, and the layer which doped p type impurity is made to form into low resistance further.

[0035] As a wafer is picked out from a reaction container after annealing and it is shown in drawing 3 , the p side contact layer 18 of the best layer and the p side clad layer 17 are \*\*\*\*\*ed by the RIE system, and it considers as the ridge configuration which has stripe width of face of 4 micrometers. Thus, by making into a stripe-like ridge configuration the layer which exists above a barrier layer, luminescence of a barrier layer comes to concentrate on the bottom of a stripe ridge, and a threshold falls. It is desirable to make into a ridge configuration a 17 or more p side clad layers [ which consist especially of strained super lattice layers ] layer.

[0036] The p electrode 21 which consists of nickel/Au is formed in the ridge maximum front face of the p side contact layer 18 in the shape of a stripe after ridge formation, the insulator layer 25 which becomes a nitride semiconductor layer's on the front faces of the maximum other than p electrode 21 from SiO<sub>2</sub> is formed, and p pad electrode 22 which connected with the p electrode 21 electrically through this insulator layer 25 is formed.

[0037] The wafer which formed p electrode as mentioned above is transported to polish equipment, polish removes silicon on sapphire, and the front face of the GaN substrate 10 is exposed. The n electrode 23 of the

exposed GaN substrate front face which becomes the whole surface from Ti/aluminum is formed mostly.

[0038] A cleavage is carried out by the Mth page (field which is equivalent to the side of a hexagonal prism when a nitride semiconductor is approximated by hexagonal system) of the GaN substrate after electrode formation, and the dielectric multilayer which becomes the cleavage plane from SiO<sub>2</sub> and TiO<sub>2</sub> is formed, and finally, in a direction parallel to p electrode, a bar is cut and it considers as a laser element.

[0039] When this laser chip was installed in the heat sink by the face up (state which the substrate and the heat sink countered), wire bonding of each electrode was carried out and laser oscillation was tried at the room temperature, in the room temperature, by threshold current density 2.0 kA/cm<sup>2</sup> and threshold-voltage 4.0V, continuous oscillation with an oscillation wavelength of 405nm was checked, and the life of 1000 hours or more was shown.

[0040]

[Effect of the Invention] Thus, in the nitride semiconductor device of this invention, an output can be sharply raised by making the layer which carried out the inclination dope of the p type impurity intervene between the nitride semiconductor layer which doped many p type impurities on a barrier layer, and the nitride semiconductor layer which doped many p type impurities. Moreover, the element of this invention can be used for many electron devices using a nitride semiconductor not only like Light Emitting Diode and a luminescence device like LD but other light-receiving devices.

[Brief Description of the Drawings]

[Drawing 1] The type section view showing the structure of the 1Light-Emitting-Diode element concerning one example of this invention.

[Drawing 2] The distribution map showing p type high impurity concentration of the Light Emitting Diode element of drawing 1.

[Drawing 3] The type section view showing the structure of LD element concerning other examples of this invention.

[Description of Notations]

1 ... Substrate

2 ... Buffer layer

3 ... The n side contact layer

- 4 ... Barrier layer
- 5 ... The 1st p side nitride semiconductor layer
- 6 ... The 2nd p side nitride semiconductor layer
- 7 ... The 3rd p side nitride semiconductor layer
- 8 ... p electrode
- 9 ... Pad electrode
- 10 ... n electrode

Fig. 1

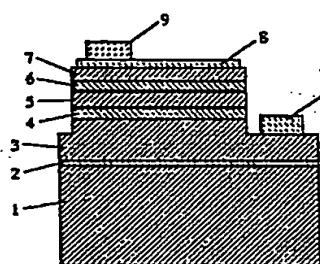


Fig. 2

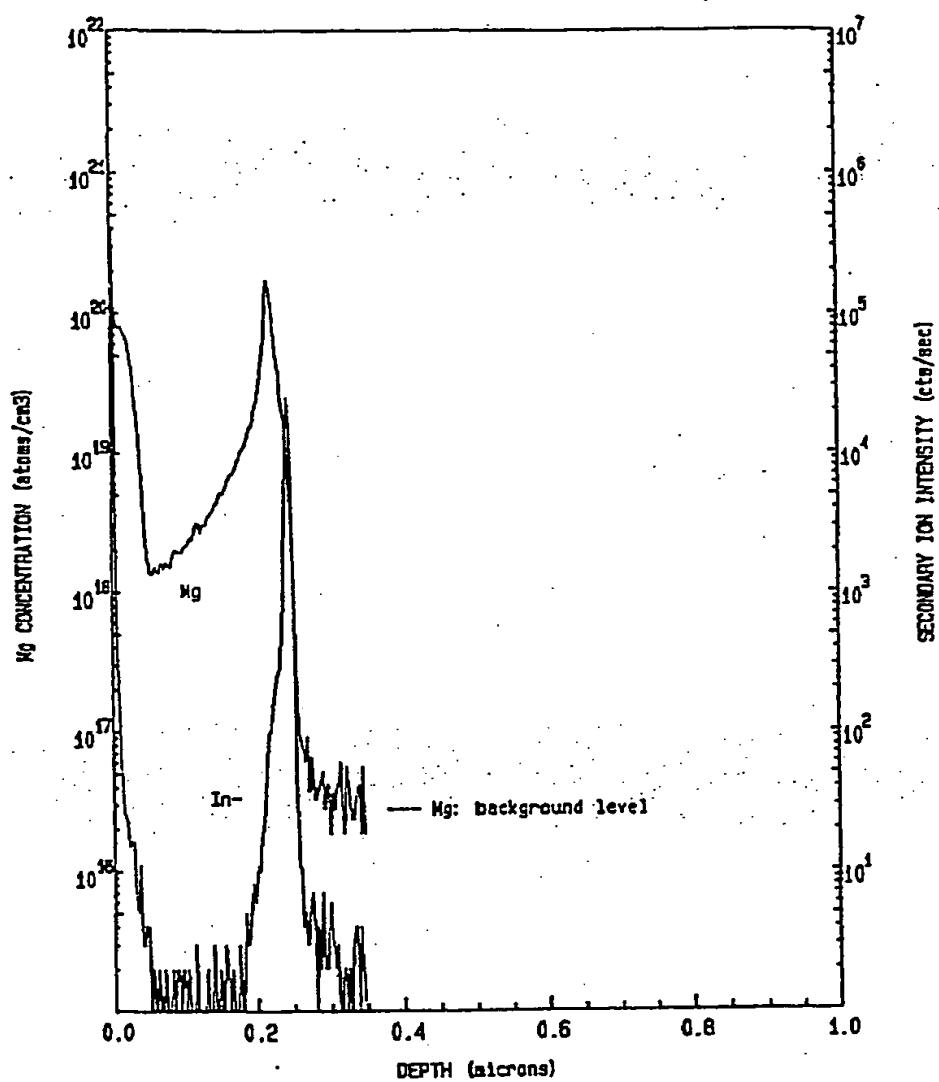
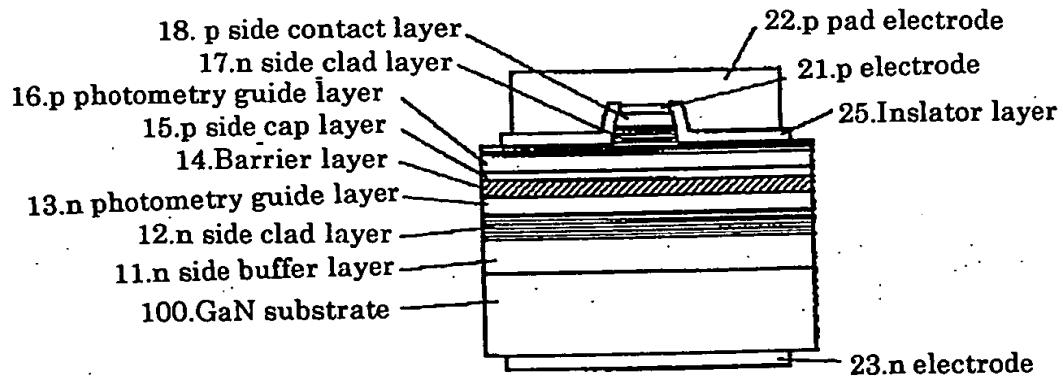


Fig. 3



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**MACHINE-ASSISTED TRANSLATION (MAT):**

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導体の成長方法

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Nitride semiconductor element and the growth  
method of a nitride semiconductor

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## (57) 【要約】

## (57)[SUMMARY]

## 【目的】

新規な窒化物半導体素子の構造と、その窒化物半導体素子を構成する窒化物半導体の成長方法とを提供することにより、LED、LDの出力を向上させる。

## [OBJECT]

The output of LED and LD is improved by providing a structure of a novel nitride semiconductor element, and the growth method of the nitride semiconductor which comprises the nitride semiconductor element.

## 【構成】

活性層上部に p 型不純物を含む第 1 の窒化物半導体層が形成され、その第 1 の窒化物半導体層上部に、その第 1 の窒化物半導体層から離れるに従って p 型不純物濃度が次第に少なくなっている第 2 の窒化物半導体層を備え、その第 2 の窒化物半導体層上部に、第 2 の窒化物半導体層の平均 p 型不純物濃度よりも多量の p 型不純物を含む第 3 の窒化物半導体層を有する。

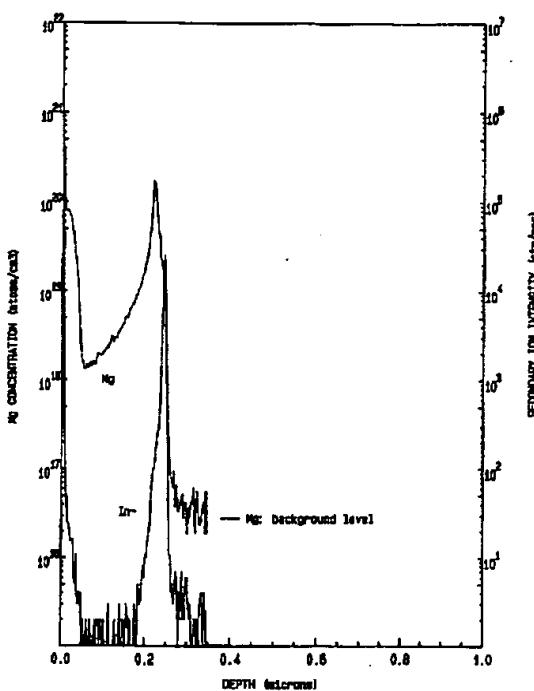
## [SUMMARY OF THE INVENTION]

The first nitride semiconductor layer which contains a p-type impurity in the active layer upper part is formed.

The 2nd nitride semiconductor layer whose p-type impurity concentration is decreasing gradually as it separates from the first nitride semiconductor layer is provided for in the first nitride semiconductor layer upper part.

The third nitride semiconductor layer containing a lot of p-type impurities than the an average of p type impurity concentration of a 2nd nitride semiconductor layer is provided for the 2nd nitride semiconductor layer upper part.

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## 【特許請求の範囲】

## [CLAIMS]

## 【請求項 1】

活性層上部に p 型不純物を含む第 1 の窒化物半導体層が形成され、その第 1 の窒化物半導体層上部に、その第 1 の窒化物半導体層から離れるに従って p 型不純物濃度が次第に少なくなっている第 2 の窒化物半導体層を備え、その第 2 の窒化物半導体層上部に、第 2 の窒化物半導体層の平均 p 型不純物濃度よりも多量の p 型不純物を含む第 3 の窒化物半導体層を有することを特徴とする窒化物半導体素子。

## [CLAIM 1]

A nitride semiconductor element, in which the first nitride semiconductor layer which contains a p-type impurity in the active layer upper part is formed.

The first nitride semiconductor layer upper part is equipped with the 2nd nitride semiconductor layer whose p-type impurity concentration is decreasing gradually as it separates from the first nitride semiconductor layer.

In the 2nd nitride semiconductor layer upper part, it has a third nitride semiconductor layer containing a lot of p-type impurities than the an average of p type impurity concentration of a 2nd nitride semiconductor layer.

## 【請求項 2】

前記第 2 の窒化物半導体層が複数の窒化物半導体層が積層され

## [CLAIM 2]

A nitride semiconductor element given in Claim 1, in which a second nitride semiconductor layer consists of the multilayer membrane with which

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た多層膜よりなり、その多層膜のp型不純物が段階的に少なくなっていることを特徴とする請求項1に記載の窒化物半導体素子。

### 【請求項3】

反応容器内において、p型不純物源ガスと、III族源ガスと、窒素源ガスとを用い、p型不純物を含む第1の窒化物半導体層を成長させた後、p型不純物源と、III族源ガスと、窒素源ガスとを用いて第2の窒化物半導体層を成長させ、第2の窒化物半導体成長中にp型不純物源ガスの流量を徐々に減らすことにより、第2の窒化物半導体層中のp型不純物濃度を第1の窒化物半導体層から離れるに従って少なくなるようにすることを特徴とする窒化物半導体の成長方法。

several nitride semiconductor layer was laminated.

The p-type impurity of the multilayer membrane has decreased stepwise.

### [CLAIM 3]

A growth method of the nitride semiconductor, in which in the reaction container, source gas of a p-type impurity, source gas of the group III, and source gas of nitrogen are used. After growing up the first nitride semiconductor layer containing a p-type impurity, a 2nd nitride semiconductor layer is grown up by using the source of a p-type impurity, source gas of the group III, and source gas of nitrogen.

The flow rate of source gas of a p-type impurity is gradually reduced in the 2nd nitride semiconductor growth. It is made to decrease the p-type impurity concentration in a 2nd nitride semiconductor layer as it separates from a first nitride semiconductor layer.

### 【発明の詳細な説明】

### [DETAILED DESCRIPTION OF INVENTION]

#### 【0001】

#### [0001]

### 【産業上の利用分野】

本発明は例えばLED、LD等の発光素子、太陽電池、光センサー等の受光素子等に用いられる窒化物半導体( $In_xAl_{1-x}Ga_yN$ 、 $0 \leq X, Y \leq 1, X+Y \leq 1$ )よりなる素子と、その素子を構成する窒化物半導体の成長方法に関する。

### [INDUSTRIAL APPLICATION]

This invention relates to the element which consists of the nitride semiconductor ( $In_xAl_{1-X}Ga_yN$ ,  $0 \leq X, Y \leq 1, X+Y \leq 1$ ) used, for example, for light receiving elements, such as a LED and LD etc. light-emitting element, a solar battery, and a photosensor, etc., and the growth method of the nitride semiconductor which composes the element.

#### 【0002】

#### [0002]

### 【従来の技術】

### [PRIOR ART]

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窒化物半導体は高輝度青色LED、純緑色LEDの材料として、本出願人により、フルカラーLEDディスプレイ、交通信号等で実用化されたばかりである。これらの各種デバイスに使用されるLEDは、n型窒化物半導体層とp型窒化物半導体層との間に、単一量子井戸構造(SQW: Single-Quantum-Well)のInGaNよりなる活性層が挟まれたダブルヘテロ構造を有している。青色、緑色等の波長はInGaN活性層のIn組成比を増減することで決定されている。青色LEDは20mAにおいて発光波長450nm、半値幅20nm、光度2cd、光出力5mW、外部量子効率9.1%である。一方、緑色LEDは同じく20mAにおいて、発光波長525nm、半値幅30nm、光度6cd、光出力3mW、外部量子効率6.3%である。

### 【0003】

また本出願人は、最近この材料を用いてパルス電流下、室温での410nmのレーザ発振を世界で初めて発表した(例えば、Jpn.J.Appl.Phys.35(1996)L74、Jpn.J.Appl.Phys.35(1996)L217等)。このレーザ素子は、InGaNを用いた多重量子井戸構造の活性層を有するダブルヘテロ構造を有し、パルス幅2μs、パルス周期2msの条件で、閾値電流610mA、閾値電流密度8.7kA/cm<sup>2</sup>、410nmの発振を示す。改良したレーザ素子もまた、Appl.Phys.Lett.69(1996)1477

The nitride semiconductor was just utilized by this applicant by the full-color LED display, the traffic signal, etc. as material of the high-intensity blue LED and the pure green LED.

LED used to these various devices has the double heterostructure in which the active layer which consists of InGaN of the single quantum well structure (SQW:Single-Quantum-Well) was pinched between a n-type nitride semiconductor layer and a p-type nitride semiconductor layer.

Wavelengths, such as blue and green, are determined by fluctuating in composition ratio of InGaN active layer.

As for blue LED, it is 450 nm in light emission wavelength in 20mA, the half value width of 20 nm, the luminous intensity of 2 cds, 5 mW of optical powers, and 9.1% of external quantum efficiencies.

On the other hand, as for green LED, similarly in 20mA, it is the light emission wavelength of 525 nm, the half value width of 30 nm, the luminous intensity of 6 cds, 3 mW of optical powers, and 6.3% of external quantum efficiencies.

### [0003]

Moreover this applicant announced recently the 410 nm laser oscillation at a room temperature in a pulse current using this material for the first time in the world (for example, Jpn.J.Appl.Phys.35(1996) L74, Jpn.J.Appl.Phys.35(1996) L217 etc.).

This laser element has the double heterostructure which has the active layer of the multiquantum well structure using InGaN.

On the conditions of 2 microns//micro-s pulse width and 2ms of pulse period, 610mA of threshold current, 8.7kA/cm-squared threshold current density, 410 nm of oscillation are shown.

The improved laser element was also announced in Appl.Phys.Lett.69 (1996) 1477.

This laser element has the structure where the ridge stripe was formed in a part of p-type nitride semiconductor layer.

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において発表した。このレーザ素子は、p型窒化物半導体層の一部にリッジストライプが形成された構造を有しており、パルス幅 $1\text{ }\mu\text{ s}$ 、パルス周期 $1\text{ m s}$ 、デューティー比 $0\text{. }1\%$ で、閾値電流 $1\text{. }8\text{. }7\text{ mA}$ 、閾値電流密度 $3\text{ k A/cm}^2$ 、 $4\text{. }1\text{. }0\text{ nm}$ の発振を示す。さらに本出願人は室温での連続発振にも初めて成功し、発表した。{例えば、日経エレクトロニクス 1996年12月2日号 技術速報、Appl.Phys.Lett.69(1996)3034、Appl.Phys.Lett.69(1996)4056等}、このレーザ素子は $20^\circ\text{C}$ において、閾値電流密度 $3\text{. }6\text{ k A/cm}^2$ 、閾値電圧 $5\text{. }5\text{ V}$ 、 $1\text{. }5\text{ mW}$ 出力において、 $27$ 時間の連続発振を示す。

【0004】

[0004]

### 【発明が解決しようとする課題】

このように窒化物半導体を用いた発光デバイスはLEDとして既に実用化されているが、未だ不十分な点もあり、さらなる発光出力の向上が望まれている。またLDは実用化を目指して現在鋭意研究中であり、出力の向上はもちろんのこと、長寿命化が望まれている。これらLED、LDのような発光デバイスの発光出力を向上させることができれば、類似した構造を有する太陽電池、光センサー等の受光デバイスの受光効率も同時に向上させることができる。従って、本発明はこのような事情を鑑み

### [PROBLEM ADDRESSED]

The light emission device thus using the nitride semiconductor is already utilized as LED.

However, there is also a still inadequate point.

The improvement in the further light emission output is desired.

Moreover LD is under research zealously currently aiming at utilization.

The improvement in output, of course, and the long life are desired.

If the light emission output of these light emission devices like LED and LD can be improved, the light-receiving efficiency of light-receiving devices, such as the solar battery which has the structure which was similar, and a photosensor, can also be improved simultaneously.

Therefore, this invention is accomplished in view of such a situation.

The purpose mainly is to improve the output

It is 1 microns//micro-s pulse width, 1ms of pulse periods, and 0.1% of duty ratios. 187mA of threshold currents, 3kA/cm-squared threshold current density, and 410 nm oscillation are shown.

Furthermore this applicant succeeded also in the continuous oscillation in a room temperature for the first time, and published {for example, Nikkei electronics Number for December 2nd, 1996 Technical news flash, Appl.Phys.Lett.69 (1996), 3034, Appl.Phys.Lett.69 (1996) 4056}. This laser element at 20 degree C, in 3.6kA/cm-squared threshold current density, threshold voltage 5.5V, and 1.5 mW output, the continuous oscillation of 27 hours is shown.

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て成されたものであって、その目的とするところは、新規な窒化物半導体素子の構造と、その窒化物半導体素子を構成する窒化物半導体の成長方法などを提供することにより、主としてLED、LDの出力を向上させることがある。

#### 【0005】

**【課題を解決するための手段】**  
 本発明の窒化物半導体素子は、活性層上部にp型不純物を含む第1の窒化物半導体層が形成され、その第1の窒化物半導体層上部に、その第1の窒化物半導体層から離れるに従ってp型不純物濃度が次第に少なくなっている第2の窒化物半導体層を備え、その第2の窒化物半導体層上部に、第2の窒化物半導体層の平均p型不純物濃度よりも多い量のp型不純物を含む第3の窒化物半導体層を有することを特徴とする。なお本発明において、活性層と第1の窒化物半導体層とは接して形成されていなくても良く、また第1の窒化物半導体層と、第2の窒化物半導体層とは接して形成されていなくても良く、さらに第2の窒化物半導体層と第3の窒化物半導体層とは接して形成されていなくても良い。

#### 【0006】

さらに本発明の窒化物半導体素子は、前記第2の窒化物半導体層が複数の窒化物半導体層が積層された多層膜となり、その

of LED and LD by providing the structure of a novel nitride semiconductor element, and the growth method of the nitride semiconductor which composes the nitride semiconductor element.

#### [0005]

#### **[SOLUTION OF THE INVENTION]**

As for the nitride semiconductor element of this invention, the first nitride semiconductor layer which contains a p-type impurity in the active layer upper part is formed. The first nitride semiconductor layer upper part is equipped with the 2nd nitride semiconductor layer whose p-type impurity concentration is decreasing gradually as it separates from the first nitride semiconductor layer.

It has the third nitride semiconductor layer which contains the p-type impurity of more quantity than the an average of p type impurity concentration of a 2nd nitride semiconductor layer in the 2nd nitride semiconductor layer upper part.

It is characterized by the above-mentioned.

In addition in this invention, an active layer and a first nitride semiconductor layer may not be formed by contacting each other. Moreover a first nitride semiconductor layer and a 2nd nitride semiconductor layer may not be formed by contacting each other. Furthermore a 2nd nitride semiconductor layer and a third nitride semiconductor layer may not be formed by contacting each other.

#### [0006]

Furthermore as for the nitride semiconductor element of this invention, the second nitride semiconductor layer consists of the multilayer membrane with which several nitride semiconductor layer was laminated.

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多層膜の p 型不純物が段階的に少なくなっていることを特徴とする。

The p-type impurity of the multilayer membrane has decreased stepwise.  
It is characterized by the above-mentioned.

### [0007]

本発明の窒化物半導体の成長方法は、反応容器内において、p型不純物源ガスと、III族源ガスと、窒素源ガスとを用い、p型不純物を含む第1の窒化物半導体層を成長させた後、p型不純物源と、III族源ガスと、窒素源ガスとを用いて第2の窒化物半導体層を成長させ、第2の窒化物半導体成長中にp型不純物源ガスの流量を徐々に減らすことにより、第2の窒化物半導体層中のp型不純物濃度を第1の窒化物半導体層から離れるに従つて少なくなるようにすることを特徴とする。

### [0007]

As for the growth method of the nitride semiconductor of this invention, in the reaction container, source gas of a p-type impurity, source gas of the group III, and source gas of nitrogen are used. After growing up the first nitride semiconductor layer containing a p-type impurity, a 2nd nitride semiconductor layer is grown up using the source of a p-type impurity, source gas of the group III, and source gas of nitrogen.

It is made to decrease the p-type impurity concentration in a 2nd nitride semiconductor layer by reducing gradually the flow rate of source gas of a p-type impurity in the 2nd nitride semiconductor growth as it separates from a first nitride semiconductor layer.

It is characterized by the above-mentioned.

### [0008]

### [0008]

**【発明の実施の形態】**  
図1は本発明の一実施例に係る窒化物半導体素子の構造を示す模式的な断面図であり、具体的にはLED素子の構造を示している。素子構造としては、サファイアよりなる基板1の上に、GaNよりなるバッファ層2、SiドープGaNよりなるn側コンタクト層3(兼n側クラッド層)、膜厚30オングストロームの単一量子井戸構造のInGaNよりなる活性層4、MgドープAlGaNよりなる第1のp側窒化物半導体層5、Mgが傾斜ドープされたGaNよりなる第2のp側窒化物半導体層

### [Embodiment]

Figure 1 is a typical sectional drawing showing the structure of the nitride semiconductor element based on one Example of this invention.

The structure of LED element is shown specifically.

As the element structure, on the substrate 1 which consists of sapphire, the buffer layer 2 which consists of GaN, n side contact layer 3 (and n side clad layer) which consists of Si dope GaN, the active layer 4 which consists of InGaN of the single quantum well structure of 30A film thickness, the first p-type nitride semiconductor layer 5 which consists of Mg dope AlGaN, 2nd p-type nitride semiconductor layer 6 which Mg becomes from GaN by which inclination dope was carried out, and the third p-type nitride semiconductor layer 7 which consists of GaN

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6、Mg 平均濃度が第2のp側窒化物半導体層6よりも多くドープされたGaNよりなる第3のp側窒化物半導体層7が積層されてなっている。第3のp側窒化物半導体層7のほぼ全面には、透光性の金属薄膜よりなるp電極8が形成され、その全面電極8の隅部にはボンディング用のパッド電極9が形成されている。一方p側窒化物半導体層側からエッチングして露出されたn側コンタクト層3の表面にはn電極10が形成されている。

#### 【0009】

また、図2にこのLED素子をSIMS(二次イオン質量分析装置)により分析したデータを示す。Mgは濃度を示し、Inは二次イオン強度でもって示している。つまりInピークは活性層の位置を示し、Mgは活性層よりもp層側に分布していることを示している。この図では最上層からCsイオンでLED素子をスパッタして、出てくる元素を分析し、横軸に深さ、縦軸にMg濃度と、In強度をとつて示している。このように、本発明の素子では、Mg濃度が活性層から離れるに従って次第に小さくなるように調整された窒化物半導体層を有している。

#### 【0010】

本発明の素子ではp型不純物を含む第1の窒化物半導体層5の上に、p型不純物が傾斜ドープされた第2のp側窒化物半導体層6を有している。この第2の

which is doped so that Mg average concentration is higher than 2nd p-type nitride semiconductor layer 6 are piled up.

On almost whole surface of the third p-type nitride semiconductor layer 7, the p electrode 8 which consists of the metal thin film of a permeability is formed. The pad electrode 9 for bonding is formed in the corner of the whole surface electrode 8.

On the other hand, the n electrode 10 is formed in the surface of n side contact layer 3 exposed by etching from a p-type nitride semiconductor layer side.

#### [0009]

Moreover, the data which analyzed this LED element by SIMS (secondary ion mass spectroscopy apparatus) are shown in Figure 2.

Mg shows concentration.

Secondary ionic strength has and shows In.

In other words, In peak shows the position of an active layer.

It is shown that Mg is distributed over a p layers side from an active layer.

In this figure, the spatter of the LED element is carried out with Cs ion from uppermost layer.

The element which comes out is analyzed.

The depth is taken as a horizontal axis and Mg concentration and In intensity are taken as a vertical axis.

Thus, with the element of this invention, it has the nitride semiconductor layer adjusted so that it might become small gradually as Mg concentration separates from an active layer.

#### [0010]

In the element of this invention, it has 2nd p-type nitride semiconductor layer 6 by which inclination dope of the p-type impurity was carried out, on the first nitride semiconductor layer 5 containing a p-type impurity.

By carrying out inclination dope of the p side

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p側窒化物半導体層はこのようにp側不純物が傾斜ドープされることによって、発光素子出力を向上させることができる。即ち、コンタクト層として作用するp型不純物が高濃度にドープされた第3のp側窒化物半導体と、その第3のp側窒化物半導体層よりも活性層に接近した位置に、p型不純物が傾斜ドープされた第2のp側窒化物半導体、さらに第2の窒化物半導体よりも活性層に接近した位置にp型不純物が高濃度にドープされた第1のp側窒化物半導体とを備えることにより、コンタクト層側から注入されるキャリアを、活性層に貯まりやすくするために、素子全体の出力を向上させることができる。

#### 【0011】

活性層4は少なくともInを含む窒化物半導体層を含む単一量子井戸構造、若しくは多重量子井戸構造とする。井戸層は膜厚100オングストローム以下、さらに好ましくは70オングストローム以下の $In_{n_x}Ga_{1-x}N$  ( $0 < X \leq 1$ )で構成することが望ましく、また障壁層は井戸層よりもバンドギャップエネルギーが大きい $In_yGa_{1-y}N$  ( $0 \leq Y <$ )、若しくは $Al_xGa_{1-x}N$  ( $0 < X' \leq 1$ )を200オングストローム以下、さらに好ましくは150オングストローム以下の膜厚で構成することが望ましい。

#### 【0012】

第1のp側窒化物半導体層5は

impurity in this way, this 2nd p-type nitride semiconductor layer can improve light-emitting element output.

Namely, the third p side nitride semiconductor with which the p-type impurity effected as a contact layer was doped in high concentration, the 2nd p side nitride semiconductor with which inclination dope of the p-type impurity was carried out at the position which approached the active layer from the third p-type nitride semiconductor layer, and furthermore the first p side nitride semiconductor with which the p-type impurity was doped in high concentration by the position which approached the active layer from the 2nd nitride semiconductor are provided. Since the carrier injected from a contact layer side can be stored easily on an active layer, the output of the whole element can be improved.

#### [0011]

An active layer 4 is taken as the single quantum well structure containing the nitride semiconductor layer which contains In at least, or a multiquantum well structure.

It is desirable to compose a well layer from  $In_xGa_1-XN$  ( $0 < X \leq 1$ ) of 100A or less (more preferably 70A or less) film thickness. Moreover it is desirable to compose a barrier layer from  $In_yGa_{1-Y}N$  ( $0 = < Y <$ ) with a band gap energy larger than a well layer, or  $Al_xGa_{1-X'}N$  ( $0 < X' \leq 1$ ) in a film thickness 200A or less, more preferably 150A or less.

#### [0012]

The first p-type nitride semiconductor layer 5

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p型不純物を含む窒化物半導体層で構成されていれば良く、特に活性層に接していても良い。半導体としては活性層よりもバンドギャップエネルギーの大きい窒化物半導体を選択し、例えば前記のように  $A_{1-x}Ga_{1-x}N$  ( $0 \leq x \leq 1$ ) を好ましく成長させる。一方ドープするp型不純物濃度は  $1 \times 10^{18}/cm^3$  以上、 $1 \times 10^{21}/cm^3$  以下、さらに好ましくは  $5 \times 10^{18}/cm^3$  以上、 $5 \times 10^{20}/cm^3$  に調整する。p型不純物としては例えばMg、Zn、Cd、Ca、Be、Sr等のII族元素を好ましくドープする。さらにこの第1の窒化物半導体層を互いに組成の異なる2種類の窒化物半導体層が積層されてなる超格子層とすることもできる。超格子層とする場合、超格子層を構成する窒化物半導体層の膜厚は100オングストローム以下、さらに好ましくは70オングストローム以下、最も好ましくは50オングストローム以下の膜厚に調整する。超格子層とすると、窒化物半導体層の結晶性が良くなり、出力がさらに向上する。超格子層とする場合、p型不純物は両方の層にドープしても良いし、いずれか一方の層にドープしても良い。

### [0013]

第2の窒化物半導体層6は第1の窒化物半導体層5に接して形成されていることが望ましいが、特に接して形成されていないても良い。例えば第1と第2の窒化物半導体層との間に数百

should just consist of the nitride semiconductor layer containing a p-type impurity.

Even if it is in contact with especially the active layer, it does not need to be.

As a semiconductor, the large nitride semiconductor of a band gap energy is selected from an active layer. For example,  $Al_xGa_{1-x}N$  ( $0 \leq x \leq 1$ ) is grown up preferably as mentioned above.

On the other hand, p-type impurity concentration to dope is adjusted to  $1 \times 10^{18}/cm^3$ - $1 \times 10^{21}/cm^3$ , more preferably  $5 \times 10^{18}/cm^3$ - $5 \times 10^{20}/cm^3$ .

As p-type impurities, for example, II group elements, such as Mg, Zn, Cd, Ca, Be, and Sr, are doped preferably.

Furthermore also let this first nitride semiconductor layer be the superlattice layer which comes to laminate 2 kinds of nitride semiconductor layers from which a composition differs mutually.

When using as a superlattice layer, the film thickness of the nitride semiconductor layer which composes a superlattice layer is adjusted to a film thickness 100A or less, more preferably 70A or less, most preferably 50A or less.

When it is a superlattice layer, the crystallinity of a nitride semiconductor layer will become better.

Output improves further.

When using as a superlattice layer, a p-type impurity may be doped in both of layers.

It may dope in any one layer.

### [0013]

Although it is desirable to form the 2nd nitride semiconductor layer 6 by contacting with the first nitride semiconductor layer 5, it does not need to form by contacting especially.

For example, the nitride semiconductor layer of the undoped of the film thickness below several hundred angstrom can also be grown

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オングストローム以下の膜厚のアンドープの窒化物半導体層を成長させることもできる。また、不純物は第3の窒化物半導体層6に接近して連続的に少なくなるように調整することが望ましいが、段階的にp型不純物のドープ量を少なくして第2の窒化物半導体層を成長させることもできる。窒化物半導体層の組成は特に問うものではないが、好ましくは第3の窒化物半導体層と同一組成とする。第2の窒化物半導体層の膜厚は $2\text{ }\mu\text{m}$ 以下、さらに好ましくは $1\text{ }\mu\text{m}$ 以下、最も好ましくは $0.5\text{ }\mu\text{m}$ 以下に調整する。また第2の窒化物半導体層を窒化物半導体の多層膜(超格子を含む)構造として、その多層膜を構成する窒化物半導体層のp型不純物濃度を段階的に少なくなるようにしても良い。

#### 【0014】

第3の窒化物半導体層7は、p電極を形成するコンタクト層とすることが望ましく、好ましくはX値が0.3以下の $\text{Al}_x\text{Ga}_{1-x}\text{N}$  ( $0 \leq X \leq 0.3$ ) するとp電極と好ましいオーミックが得られる。第3の窒化物半導体層7のp型不純物濃度は、第1の窒化物半導体層5と同じく、 $1 \times 10^{18}/\text{cm}^3$ 以上、 $1 \times 10^{21}/\text{cm}^3$ 以下、さらに好ましくは $5 \times 10^{18}/\text{cm}^3$ 以上、 $5 \times 10^{20}/\text{cm}^3$ に調整することが望ましい。また第3の窒化物半導体層の膜厚は第2の窒化物半導体層よりも薄く調整することが望ましい。即ち、コンタクト

up between first and second nitride semiconductor layers.

Moreover, although it is desirable to adjust so that the third nitride semiconductor layer 6 may be approached and it may decrease continuously as for an impurity, it can decrease stepwise the amount of dope of a p-type impurity, and can also grow up a 2nd nitride semiconductor layer.

Especially the composition of a nitride semiconductor layer does not matter.

However, preferably, it uses as the same composition as a third nitride semiconductor layer.

The film thickness of a 2nd nitride semiconductor layer is adjusted to 2 micrometers or less, more preferably 1 micrometer or less, most preferably below 0.5 micrometer.

Moreover a 2nd nitride semiconductor layer is made into the multilayer membrane (superlattice is contained) structure of a nitride semiconductor. It may be made to decrease the p-type impurity concentration of the nitride semiconductor layer which composes the multilayer membrane stepwise.

#### [0014]

As for the third nitride semiconductor layer 7, it is desirable to use as the contact layer which forms p electrode. Preferably if X value is 0.3 or less  $\text{Al}_x\text{Ga}_{1-X}\text{N}$  ( $0 \leq X \leq 0.3$ ), p electrode and a desirable ohmic will be obtained.

Like the first nitride semiconductor layer 5, it is desirable to adjust the p-type impurity concentration of the third nitride semiconductor layer 7, to  $1 \times 10^{18}/\text{cm}^3$ - $1 \times 10^{21}/\text{cm}^3$ , more preferably  $5 \times 10^{18}/\text{cm}^3$ - $5 \times 10^{20}/\text{cm}^3$ .

Moreover it is desirable to adjust the film thickness of a third nitride semiconductor layer, more thinly than a 2nd nitride semiconductor layer.

That is, the film thickness of the third p-type nitride semiconductor layer effected as a contact layer is made thin, and a p-type impurity is doped in high concentration. Since a contact resistance falls, it is in the trend that  $V_f$  (forward

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層として作用する第3のp型窒化物半導体層の膜厚を薄くして、高濃度にp型不純物をドープすることによりコンタクト抵抗が下がるので、V<sub>f</sub>（順方向電圧）が低下しやすい傾向にある。

## 【0015】

## [0015]

## 【実施例】

以下、MOCVD法を用いて本発明の窒化物半導体素子の製造方法について説明する。

## [Example]

Hereafter, the manufacturing method of the nitride semiconductor element of this invention is demonstrated using MOCVD method.

## 【0016】

## [0016]

## 【実施例1】

サファイア(0001)面を正面とする基板を用意し、原料ガスにTMG(トリメチルガリウム)、アンモニアを用いて500°CでGaNよりなるバッファ層を200オングストロームの膜厚で成長させる。

## [Example 1]

The substrate which makes a sapphire (0001) surface a main surface is prepared.

TMG(trimethyl gallium) and ammonia are used as starting material gas. The buffer layer which consists of GaN at 500 degree C is grown up by the 200A film thickness.

## 【0017】

次に温度を1050°Cに上昇させ、TMG、アンモニア、不純物ガスにモノシリランガスを用いて、Siを $1 \times 10^{18}/\text{cm}^3$ ドープしたn型GaN層を5μmの膜厚で成長させる。

## [0017]

Next temperature is risen at 1050 degree C.

Monosilane gas is used for TMG, ammonia, and impurities gas.

The n-type GaN layer which doped Si $1 \times 10^{19}/\text{cm}^3$  is grown up by the 5-micrometer film thickness.

## 【0018】

次に温度を800°Cにして、TMI(トリメチルインジウム)、TMG、アンモニアを用い、活性層として、アンドープIn<sub>0.4</sub>Ga<sub>0.6</sub>Nよりなる井戸層を25オングストロームの膜厚で成長

## [0018]

Next temperature is made into 800 degree C.

TMI(trimethyl indium), TMG, and ammonia are used. As an active layer, the well layer which consists of undoped In<sub>0.4</sub>Ga<sub>0.6</sub>N is grown up by the 25A film thickness.

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させる。

### [0019]

次に温度を1050°Cにして、TMG、アンモニア、不純物ガスとしてCp2Mg(シクロペニタジエニルマグネシウム)を用い、Mgを $1 \times 10^{20}/\text{cm}^3$ ドープしたp型Al<sub>0.3</sub>Ga<sub>0.7</sub>Nよりなる第1の窒化物半導体層を200オングストロームの膜厚で成長させる。この第1の窒化物半導体層はキャリアを閉じ込める層として作用する。

### [0020]

第1の窒化物半導体層成長後、原料ガスを止め、続いて再度TMG、アンモニア、Cp2Mgを流し、1050°Cで、p型不純物が傾斜ドープされたGaNによりなる第2の窒化物半導体層を0.18μmの膜厚で成長させる。但しCp2MgはMFC(マスフローコントローラ)により、成長中徐々に流量が少なくなるように調整し、第2の窒化物半導体が成長し終わる頃には、Cp2Mgの流量が0となるようにする。

### [0021]

第2の窒化物半導体層成長後、TMG、アンモニア、Cp2Mgを用い、Mgを $1 \times 10^{20}/\text{cm}^3$ ドープした第3の窒化物半導体層を300オングストロームの膜厚で成長させる。

### [0022]

以上のようにして窒化物半導体を成長させたウェーハを反応容

### [0019]

Next temperature is made into 1050 degree C.

TMG, ammonia, and as impurity gas, Cp2 mg (cyclopentadienyl magnesium) are used. The first nitride semiconductor layer which consists of p-type Al0.3Ga0.7N which doped Mg 1\*1020/cm3 is grown up by the 200A film thickness.

This first nitride semiconductor layer is effected as a layer which shuts up a carrier.

### [0020]

Starting material gas is stopped after first nitride semiconductor layer formation length. TMG, ammonia, and Cp2 mg are poured again continuously.

The 2nd nitride semiconductor layer which a p-type impurity becomes from GaN by which inclination dope was carried out, at 1050 degree C is grown up by the 0.18-micrometer film thickness.

However by MFC (mass flow controller), Cp2 mg is adjusted so that a flow rate may decrease gradually in the growth.

When a 2nd nitride semiconductor finishes growing, the flow rate of Cp2 mg becomes 0.

### [0021]

After a 2nd nitride semiconductor layer grows, the third nitride semiconductor layer which doped Mg 1\*1020/cm3 is grown up by the 300A film thickness using TMG, ammonia, and Cp2 mg.

### [0022]

An annealing of the wafer which thus grew up the nitride semiconductor is performed at 700 degree C in nitrogen atmosphere in the reaction

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器内において、窒素雰囲気中 700℃でアニーリングを行い、p型不純物をドープした層をさらに低抵抗化させる。アニーリング後、ウェーハを反応容器から取り出し、RIE装置により最上層の第3の窒化物半導体層側からエッチングを行い、n電極を形成すべきn側コンタクト層の表面を露出させる。最上層の第3の窒化物半導体層のほぼ全面にNi/Auよりなる全面電極を200オングストロームの膜厚で形成し、その全面電極の一部に1μmの膜厚でAuよりなるパッド電極を形成する。一方、露出させたn側コンタクト層の表面には、WとAuよりなるn電極を形成する。

#### 【0023】

以上のようにして電極を形成したウェーハを350μm角のチップに分離し、発光させたところ20mAにおいて、Vf 3.2V、発光波長525nm、光出力3.5mW、外部量子効率7.3%となり、傾斜ドープしていない従来の緑色LEDに比較して、およそ1.2倍に向上了した。

#### 【0024】

#### 【実施例2】

実施例1において、第1の窒化物半導体層成長後、原料ガスを止め、続いて再度TMG、アンモニア、Cp2Mgを流し、1050℃で、p型不純物を $1 \times 10^{19}/\text{cm}^3$ ドープしたGaN層

container.

The layer which doped the p-type impurity is made to form into a low resistance further.

A wafer is picked out from the reaction container after an annealing.

RIE apparatus performs an etching from the third nitride semiconductor layer side of uppermost layer.

The surface of n side contact layer which should form n electrode is exposed.

The whole surface electrode which the third nitride semiconductor layer of uppermost layer becomes from Ni/Au almost entirely is formed in a 200A film thickness.

The pad electrode which turns into a part of the whole surface electrode from Au by the 1-micrometer film thickness is formed.

On the other hand, n electrode which consists of W and Au is formed in the surface of exposed n side contact layer.

#### [0023]

The wafer which thus formed the electrode is separated to the chip of 350 micrometer angle. Light was made to emit light. In 20mA, it is Vf 3.2V and the light emission wavelength of 525 nm. It becomes 3.5 mW of optical powers, and 7.3% of external quantum efficiencies.

Compared with the conventional green LED which is not carrying out inclination dope, it improved by about 1.2 times.

#### [0024]

#### [Example 2]

In Example 1, after a first nitride semiconductor layer grows, starting material gas is stopped. Then TMG, ammonia, and Cp2mg are flowed again.

At 1050 degree C, 500A of GaN layers which doped the p-type impurity  $1 \times 10^{19}/\text{cm}^3$  is grown up.

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を500オングストローム成長させ、次にCp2Mgの流量を変えて、Mgを $5 \times 10^{18}/\text{cm}^3$ ドープしたGaN層を500オングストローム成長させ、次にMgを $1 \times 10^{18}/\text{cm}^3$ ドープしたGaN層を500オングストローム成長させ、最後にMgをドープしていないGaN層を500オングストローム成長させて、総膜厚0.2μmの第2の窒化物半導体層を成長させる。その他は実施例1と同様にしたところ、実施例1のものとほぼ同等の特性を有するLED素子が作製できた。

## 【0025】

Next the flow rate of Cp2 mg is changed.  
500A of GaN layers which doped Mg  
 $5 \times 10^{18}/\text{cm}^3$  is grown up.

Next 500A of GaN layers which doped Mg  
 $1 \times 10^{18}/\text{cm}^3$  is grown up.

500A of GaN layers which finally have not  
doped Mg is grown up.

The 2nd nitride semiconductor layer of the  
0.2 micrometers of the total film thicknesses is  
grown up.

When others were made to be the same as  
that of Example 1, they have produced LED  
element which has characteristics almost  
equivalent to the Example 1.

## [0025]

## 【実施例3】

図3は本発明に係る一レーザ素子の構造を示す模式的な断面図であり、以下、この図を元に本発明の第3実施例について説明する。

## [Example 3]

Figure 3 is a typical sectional drawing showing  
the structure of the 1 laser element based on  
this invention.

Hereafter, this figure is demonstrated to origin  
about the 3rd Example of this invention.

## 【0026】

サファイア(0001)面を正面とする基板の上にGaNよりなるバッファ層を介してGaNよりなる単結晶を120μmの膜厚で成長させたGaN基板100を用意する。このGaN基板100をサファイアの上に成長させた状態で、反応容器内にセットし、温度を1050°Cまで上げ、実施例1と同様にして、GaN基板100上にSiを $1 \times 10^{18}/\text{cm}^3$ ドープしたGaNよりなるn側バッファ層11を4μmの膜厚で成長させる。

## [0026]

The GaN substrate 100 where the single crystal  
which consists of GaN was grown up in the  
120-micrometer film thickness on the substrate  
which makes a sapphire (0001) surface a main  
surface, through the buffer layer which consists  
of GaN, is prepared.

In the state where it was made to grow on  
sapphire, this GaN substrate 100 is set in the  
reaction container. Temperature is raised to  
1050 degree C.

It is made to be the same as that of Example  
1.

n side buffer layer 11 which consists of GaN  
which doped Si  $1 \times 10^{18}/\text{cm}^3$  on the GaN  
substrate 100 is grown up in the 4-micrometer  
film thickness.

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このn側バッファ層は高温で成長させるバッファ層であり、例えば実施例1のように、サファイア、SiC、スピネルのように窒化物半導体と異なる材料よりなる基板の上に、900°C以下の低温において、GaN、AlN等を、0.5 μm以下の膜厚で直接成長させるバッファ層2とは区別される。

### [0027]

(n側クラッド層12=歪み超格子層) 続いて、1050°CでTMA、TMG、アンモニア、シランガスを用い、Siを $1 \times 10^{19}/\text{cm}^3$ ドープしたn型Al<sub>0.3</sub>Ga<sub>0.7</sub>Nよりなる第1の層を40オングストロームの膜厚で成長させ、続いてシランガス、TMAを止め、アンドープのGaNよりなる第2の層を40オングストロームの膜厚で成長させる。そして第1層+第2層+第1層+第2層+...というように歪み超格子層を構成し、それぞれ100層ずつ交互に積層し、総膜厚0.8 μmの歪み超格子よりなるn側クラッド層12を成長させる。

### [0028]

(n側光ガイド層13) 続いて、シランガスを止め、1050°CでアンドープGaNよりなるn側光ガイド層13を0.1 μmの膜厚で成長させる。このn側光ガイド層は、活性層の光ガイド層として作用し、GaN、InGaNを成長させることができましく、通常100オングストローム～5 μm、さらに好まし

This n side buffer layer is a buffer layer grown up at high temperature.

For example, it is different from the buffer layer 2 which grows up GaN and AlN etc. at low temperature of 900 degree C or less directly in the film thickness below 0.5 micrometer on the substrate which consists of the material which differs from a nitride semiconductor like sapphire, SiC, and a spinel, like Example 1.

### [0027]

(n side clad layer 12= distortion super-latticed layer) Then, TMA, TMG, ammonia, and silane gas are used at 1050 degree C. The first layer which consists of n-type Al<sub>0.3</sub>Ga<sub>0.7</sub>N which doped Si  $1 \times 10^{19}/\text{cm}^3$  is grown up in 40A film thickness.

Then silane gas and TMA are stopped. The 2nd layer which consists of GaN of a undoped is grown up by the 40A film thickness.

And the distortion super-latticed layer is composed like 1st layer + 2nd layer + 1st layer + 2nd layer + \*\*\*. It respectively laminates 100 layers at a time alternately. n side clad layer 12 which consists of the strained super lattice of the 0.8 micrometers of the total film thicknesses is grown up.

### [0028]

(n side light guide layer 13) Then, silane gas is stopped.

n side light guide layer 13 which consists of a undoped GaN at 1050 degree C is grown up by the 0.1-micrometer film thickness.

This n side light guide layer is effected as a light guide layer of an active layer.

It is desirable to grow up GaN and InGaN. It is desirable to usually grow in the 100A - 5 micrometers film thickness, more preferably 200A - 1 micrometer.

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くは200オングストローム～ $1\mu\text{m}$ の膜厚で成長させることができが望ましい。またこの層をアンドープの歪み超格子層とすることもできる。歪み超格子層とする場合にはバンドギャップエネルギーは活性層より大きく、n側クラッド層よりも小さくなる。

### 【0029】

(活性層14) 次に、原料ガスにTMG、TMI、アンモニアを用いて活性層14を成長させる。活性層14は温度を800°Cに保持して、アンドープIn<sub>0.2</sub>Ga<sub>0.8</sub>Nよりなる井戸層を25オングストロームの膜厚で成長させる。次にTMIのモル比を変化させるのみで同一温度で、アンドープIn<sub>0.01</sub>Ga<sub>0.95</sub>Nよりなる障壁層を50オングストロームの膜厚で成長させる。この操作を2回繰り返し、最後に井戸層を積層した総膜厚175オングストロームの多重量子井戸構造(MQW)の活性層を成長させる。活性層は本実施例のようにアンドープでもよいし、またn型不純物及び／又はp型不純物をドープしても良い。不純物は井戸層、障壁層両方にドープしても良く、いずれか一方にドープしてもよい。

### 【0030】

(p側キャップ層15=第1の窒化物半導体層) 次に、温度を1050°Cに上げ、TMG、TMA、アンモニア、Cp2Mg(シクロペンタジエニルマグネシウム)を用い、p側光ガイド層1

Moreover also this layer is made into the strained super lattice layer of a undoped.

When using as the distortion super-latticed layer, a band gap energy is larger than an active layer. It is made smaller than n side clad layer.

### [0029]

(Active layer 14) Next, TMG, TMI, and ammonia are used for starting material gas, and an active layer 14 is grown up.

An active layer 14 grows up the well layer which consists of undoped In<sub>0.2</sub>Ga<sub>0.8</sub>N, by the 25A film thickness holding temperature at 800 degree C.

Next the barrier layer which consists of undoped In<sub>0.01</sub>Ga<sub>0.95</sub>N at the same temperature is grown up in the 50A film thickness by changing molar ratio of TMI. This operation is repeated twice.

The active layer of the multiquantum well structure (MQW) of the 175A of the total film thicknesses which finally laminated the well layer is grown up.

A undoped is sufficient as an active layer like this Example.

Moreover a n-type impurity and/or a p-type impurity may be doped.

An impurity may be doped to both well layer and barrier layer. It may dope to any one.

### [0030]

(p side cap layer 15= first nitride semiconductor layer) Next, temperature is raised to 1050 degree C. TMG, TMA, ammonia, and Cp2Mg (cyclopentadienyl magnesium) are used. p side cap layer 17 which consists of p-type Al<sub>0.3</sub>Ga<sub>0.7</sub>N which has bigger band gap energy than and p side light guide layer 16 and doped

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6よりもバンドギャップエネルギーが大きい、Mgを $1 \times 10^{20}/\text{cm}^3$ ドープしたp型Al<sub>0.3</sub>Ga<sub>0.7</sub>Nよりなるp側キャップ層17を300オングストロームの膜厚で成長させる。p側キャップ層は0.5 μm以下、さらにに好ましくは0.1 μm以下の膜厚で成長させると、p側キャップ層がキャリアを活性層内に閉じ込めるためのバリアとして作用するので、出力が向上する。このp型キャップ層15の膜厚の下限は特に限定しないが、10オングストローム以上の膜厚で形成することが望ましい。

### [0031]

(p側光ガイド層16=第2の窒化物半導体層) p側キャップ層15成長後、再度TMG、Cp2Mg、アンモニアを用い、実施例1と同様にして、1050°Cで、バンドギャップエネルギーがp側キャップ層15よりも小さい、p型不純物が傾斜ドープされたGaNよりなるp側光ガイド層16を0.1 μmの膜厚で成長させる。この層は、活性層の光ガイド層として作用する。

### [0032]

(p側クラッド層17) 続いて、1050°CでMgを $1 \times 10^{20}/\text{cm}^3$ ドープしたp型Al<sub>0.3</sub>Ga<sub>0.7</sub>Nよりなる第3の層を40オングストロームの膜厚で成長させ、続いてTMAのみを止め、アンドープGaNよりなる第4の層を40オングストロームの

Mg $1 \times 10^{20}/\text{cm}^3$ は300Åの膜厚で成長する。

If p side cap layer is grown up by the film thickness below 0.5 micrometer, further preferably 0.1 micrometers or less, since it effects as a barrier for p side cap layer shutting up a carrier in an active layer, output improves.

Especially the lower limit of the film thickness of this p-type cap layer 15 does not limit.

However, it is desirable to form by the film thickness 10Å or more.

### [0031]

(p side light guide layer 16= 2nd nitride semiconductor layer) After p side cap layer 15 grows, TMG, Cp2 mg, and ammonia are used again. It is made to be the same as that of Example 1.

p side light guide layer 16 which has a band gap energy smaller than p side cap layer 15 consists of GaN which carried out inclination dope of p-type impurity, is grown up at 1050 degree C in the 0.1-micrometer film thickness.

This layer is effected as a light guide layer of an active layer.

### [0032]

(p side clad layer 17) Then, the third layer which consists of p-type Al<sub>0.3</sub>Ga<sub>0.7</sub>N which doped Mg $1 \times 10^{20}/\text{cm}^3$ , is grown up at 1050 degree C in the 40Å film thickness. Then only TMA is stopped.

The 4th layer which consists of a undoped GaN is grown up by the 40Å film thickness.

And this operation is respectively repeated 100 times. p side clad layer 17 which consists of

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膜厚で成長させる。そしてこの操作をそれぞれ100回繰り返し、総膜厚0.8 μmの歪み超格子層となるp側クラッド層17を形成する。

### [0033]

(p側コンタクト層18=第3の窒化物半導体層) 最後に、1050°Cで、p側クラッド層17の上に、Mgを $2 \times 10^{20}/\text{cm}^3$ ドープしたp型GaNによるp側コンタクト層18を150オングストロームの膜厚で成長させる。p側コンタクト層18はp型の $\text{In}_x\text{Al}_{1-x}\text{Ga}_y\text{N}$  ( $0 \leq X, Y \leq 1$ ) で構成することができ、好ましくはMgをドープしたGaNとすれば、p電極21と最も好ましいオーミック接触が得られる。またp型 $\text{Al}_y\text{Ga}_{1-y}\text{N}$ を含む歪み超格子構造のp側クラッド層17に接して、バンドギャップエネルギーの小さい窒化物半導体をp側コンタクト層として、その膜厚を500オングストローム以下と薄くしているために、実質的にp側コンタクト層18のキャリア濃度が高くなりp電極と好ましいオーミックが得られて、素子の閾値電流、電圧が低下する。

### [0034]

以上のようにして窒化物半導体を成長させたウェーハを反応容器内において、窒素雰囲気中700°Cでアニーリングを行い、p型不純物をドープした層をさらに低抵抗化させる。

the strained super lattice layer of the 0.8 micrometers of the total film thicknesses is formed.

### [0033]

(p side contact layer 18= third nitride semiconductor layer) At the end, p side contact layer 18 which consists of the p-type GaN which doped Mg  $2 \times 10^{20}/\text{cm}^3$  on p side clad layer 17, is grown up at 1050 degree C in the 150A film thickness.

p side contact layer 18 can compose p-type In $X\text{AlYGa1-X-YN}$  ( $0 \leq X, Y \leq 1$ ,  $X+Y \leq 1$ ).

GaN, then the p electrode 21 which preferably doped Mg, and most desirable ohmic contact are obtained.

Moreover p side clad layer 17 of the distortion superstructure containing p-type Al $Y\text{Ga1-YN}$  is touched.

The film thickness is made thin with 500A or less, using the small nitride semiconductor of a band gap energy as p side contact layer. Therefore, the carrier concentration of p side contact layer 18 becomes high substantially. p electrode and a desirable ohmic are obtained.

The threshold current of an element and a voltage reduce.

### [0034]

An annealing of the wafer which thus grew up the nitride semiconductor at 700 degree C in nitrogen atmosphere in the reaction container.

The layer which doped the p-type impurity is made to form into a low resistance further.

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## 【0035】

アニーリング後、ウェーハを反応容器から取り出し、図3に示すように、RIE装置により最上層のp側コンタクト層18と、p側クラッド層17とをエッチングして、4μmのストライプ幅を有するリッジ形状とする。このように、活性層よりも上部にある層をストライプ状のリッジ形状とすることにより、活性層の発光がストライプリッジの下に集中するようになって閾値が低下する。特に歪み超格子層よりなるp側クラッド層17以上の層をリッジ形状とすることが好ましい。

## [0035]

A wafer is picked out from the reaction container after an annealing.

As shown in Figure 3, p side contact layer 18 of uppermost layer and p side clad layer 17 are etched with RIE apparatus.

It considers as the ridge form where it has the stripe width of 4 micrometers.

Thus, the layer which exists above an active layer is made into stripe-like ridge form. A light emission of an active layer comes to concentrate on the bottom of a stripe ridge, and a threshold reduces.

It is desirable to make the layer of 17 or more of p side clad layers which consist especially of the distortion super-latticed layer into ridge form.

## 【0036】

リッジ形成後、p側コンタクト層18のリッジ最表面にNi/Auよりなるp電極21をストライプ状に形成し、p電極21以外の最表面の窒化物半導体層のにSiO<sub>2</sub>よりなる絶縁膜25を形成し、この絶縁膜25を介してp電極21と電気的に接続したpパッド電極22を形成する。

## [0036]

After carrying out ridge formation, the p electrode 21 which becomes the ridge outermost surface of p side contact layer 18 from Ni/Au is formed stripe-like.

The insulating film 25 which becomes the nitride semiconductor layer's of outermost surfaces other than p electrode 21 from SiO<sub>2</sub> is formed. The p electrode 21 and electrically connected p pad electrode 22 are formed through this insulating film 25.

## 【0037】

以上のようにして、p電極を形成したウェーハを研磨装置に移送し、サファイア基板を研磨により除去し、GaN基板10の表面を露出させる。露出したGaN基板表面のほぼ全面にTi/Alよりなるn電極23を形成する。

## [0037]

It is made above.

The wafer that thus formed p electrode is transferred to a polish apparatus. A sapphire substrate is removed by the sanding. The surface of the GaN substrate 10 is exposed.

The n electrode 23 of exposed GaN substrate surface which consists of Ti/Al almost entirely is formed.

## 【0038】

電極形成後GaN基板のM面

## [0038]

After forming an electrode, it cleaves by M sides

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(窒化物半導体を六方晶系で近似した場合に六角柱の側面に相当する面)で劈開し、その劈開面に  $\text{SiO}_2$  と  $\text{TiO}_2$  よりなる誘電体多層膜を形成し、最後に p 電極に平行な方向で、バーを切断してレーザ素子とする。

(side which is equivalent to the side of a hexagonal column when approximating a nitride semiconductor by the hexagonal system) of GaN substrate.

The dielectric multilayer membrane which becomes the cleavage plane from  $\text{SiO}_2$  and  $\text{TiO}_2$  is formed.

Finally, in a direction parallel to p electrode, a bar is cut and it makes a laser element.

### [0039]

このレーザチップをフェースアップ（基板とヒートシンクとが対向した状態）でヒートシンクに設置し、それぞれの電極をワイヤーボンディングして、室温でレーザ発振を試みたところ、室温において、閾値電流密度  $2.0 \text{ kA/cm}^2$ 、閾値電圧  $4.0 \text{ V}$  で、発振波長  $405 \text{ nm}$  の連続発振が確認され、1000時間以上の寿命を示した。

### [0039]

This laser chip is installed to a heat sink with face up (in the state where the substrate and the heat sink oppositely faced).

The wire bonding of each electrode was carried out, and the laser oscillation was tried at the room temperature. At a room temperature, it is  $2.0 \text{kA/cm}^2$ -squared threshold current density. It is threshold voltage  $4.0\text{V}$ . A continuous oscillation with an oscillation wavelength of  $405 \text{ nm}$  is confirmed.

Or more of the life span was shown for 1000 hours.

### [0040]

### [0040]

#### 【発明の効果】

このように、本発明の窒化物半導体素子では、活性層の上にある p 型不純物を多くドープした窒化物半導体層と、p 型不純物を多くドープした窒化物半導体層との間に、p 型不純物を傾斜ドープした層を介在させることにより、出力が大幅に向上させることができる。また本発明の素子は LED、LD のような発光デバイスだけではなく、他の受光デバイスのような窒化物半導体を用いた多くの電子デバイスに用いることができる。

#### [EFFECT OF THE INVENTION]

Thus, in the nitride semiconductor element of this invention, output can be sharply improved by interposing the layer which carried out inclination dope of the p-type impurity between the nitride semiconductor layer which doped many p-type impurity on an active layer, and the nitride semiconductor layers which doped many p-type impurity.

Moreover the element of this invention can be used for not only like not only the light emission device like LED and LD, but many electronic device using the nitride semiconductor such as the other light-receiving device.

#### 【図面の簡単な説明】

#### [BRIEF EXPLANATION OF DRAWINGS]

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**【図 1】**

本発明の一実施例に係る一LED素子の構造を示す模式断面図。

**【図 2】**

図1のLED素子のp型不純物濃度を示す分布図。

**【図 3】**

本発明の他の実施例に係るLD素子の構造を示す模式断面図。

**【符号の説明】**

- 1 . . . 基板
- 2 . . . バッファ層
- 3 . . . n側コンタクト層
- 4 . . . 活性層
- 5 . . . 第1のp側窒化物半導体層
- 6 . . . 第2のp側窒化物半導体層
- 7 . . . 第3のp側窒化物半導体層
- 8 . . . p電極
- 9 . . . パッド電極
- 10 . . . n電極

**【図 1】****[FIGURE 1]**

Model sectional drawing showing the structure of the 1LED element based on one Example of this invention.

**[FIGURE 2]**

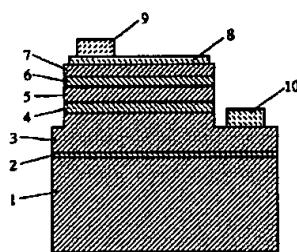
The distribution figure showing the p-type impurity concentration of LED element of Figure 1.

**[FIGURE 3]**

Model sectional drawing showing the structure of LD element based on the other Example of this invention.

**[EXPLANATION OF DRAWING]**

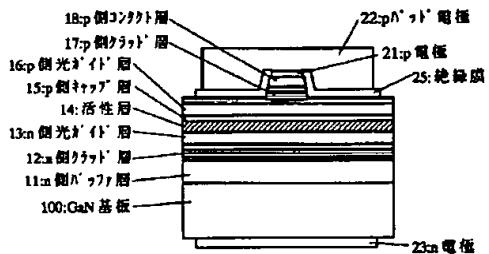
- 1\*\*\* substrate
- 2\*\*\* buffer layer
- 3\*\*\*n side contact layer
- 4\*\*\* active layer
- 5\*\*\* first p-type nitride semiconductor layer
- 6\*\*\* 2nd p-type nitride semiconductor layer
- 7\*\*\* third p-type nitride semiconductor layer
- 8\*\*\*p electrode
- 9\*\*\* pad electrode
- 10\*\*\*n electrode

**[FIGURE 1]**

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【図 3】

[FIGURE 3]

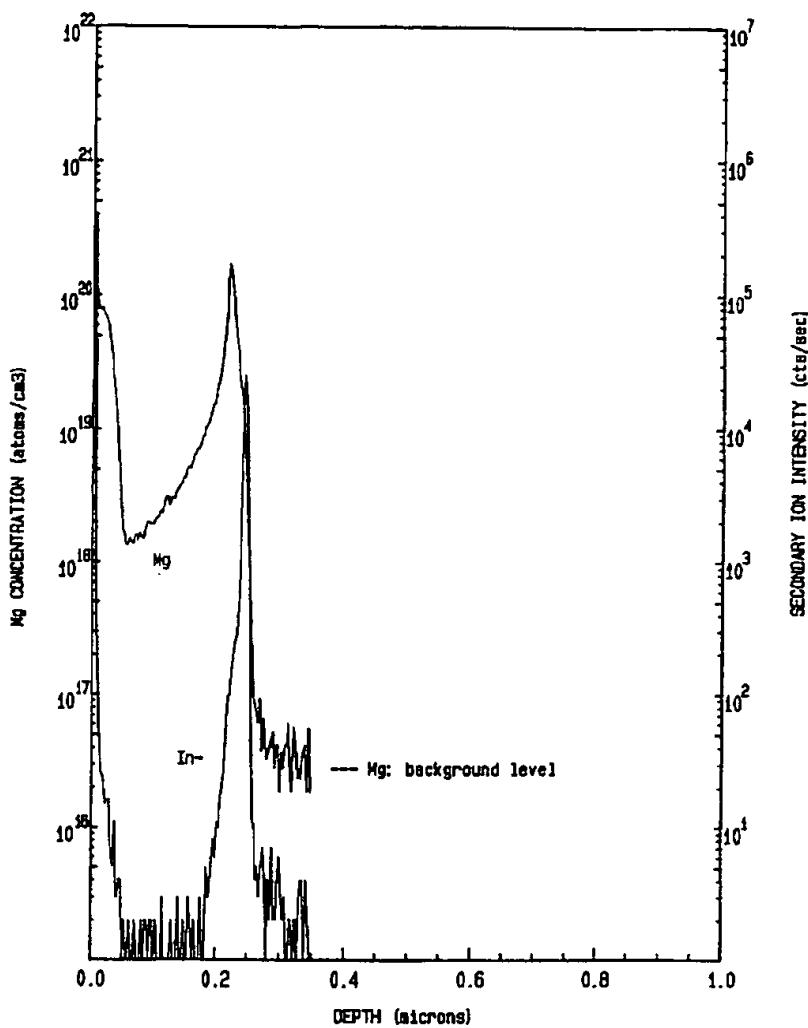


- 11: n-type buffer layer
- 12: n-type clad layer
- 13: n-type light guide layer
- 14: active layer
- 15: p-type cap layer
- 16: p-type light guide layer
- 17: p-type clad layer
- 18: p-type contact layer
- 21: p electrode
- 22: p pad electrode
- 23: n electrode
- 25: insulating film
- 100:GaN substrate

【図 2】

[FIGURE 2]

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